AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims .

1-25. (Cancelled)

26. (New) A comparator offset calibration method for A/D converters, comprising the steps of:

providing, for each comparator in a comparator array, a common reference signal to both comparator input terminals;

forcing each comparator in said array into the same predetermined logical output state; and

adjusting, for each comparator in said array, the comparator trip-point until the logical output state is inverted.

27. (New) The method of claim 26, further comprising the step of adjusting each comparator trip-point by a monotonically varying signal.

28. (New) The method of claim 26, further comprising the step of simultaneously adjusting all comparators in said array by a common ramp signal.

29. (New) The method of claim 26, further comprising the step of D/A converting, for each comparator in said array, a digital ramp signal into an analog trip-point adjustment signal.

30. (New) The method of claim 29, further comprising the step of storing, for each comparator in said array, an offset calibration coefficient representing the digital ramp signal value that inverts its logical output state.

31. (New) The method of claim 29, further comprising the step of storing, for each comparator in said array, an offset calibration coefficient representing

the average of an increasing digital ramp signal value that inverts its logical output state and a decreasing digital ramp signal value that inverts its logical output state.

32. (New) The method of claim 29, further comprising the steps of:

repeating, for each comparator in said array, said adjustment step; and

storing, for each comparator in said array, an offset calibration coefficient representing the average of several digital ramp signal values that invert its logical output state.

33. (New) The method of claim 30, further comprising the step of storing, for each comparator in said array, said offset calibration value externally at A/D converter power-down for later retrieval at A/D converter startup.

34. (New) A comparator offset calibration system for A/D converters, comprising:

means for providing, for each comparator in a comparator array, a common reference signal to both comparator input terminals;

means for forcing each comparator in said array into the same predetermined logical output state; and

means for adjusting, for each comparator in said array, the comparator trip-point until the logical output state is inverted.

35. (New) The system of claim 34, further comprising means for adjusting each comparator trip-point by a monotonically varying signal.

36. (New) The system of claim 34, further comprising means for simultaneously adjusting all comparators in said array by a common ramp signal.

37. (New) The system of claim 34, further comprising means for D/A converting, for each comparator in said array, a digital ramp signal into an analog trip-point adjustment signal.

38. (New) The system of claim 37, further comprising registers for storing, for each comparator in said array, an offset calibration coefficient representing the digital ramp signal value that inverts its logical output state.

39. (New) The system of claim 37, further comprising registers for storing, for each comparator in said array, an offset calibration coefficient representing the average of an increasing digital ramp signal value that inverts its logical output state and a decreasing digital ramp signal value that inverts its logical output state.

40. (New) The system of claim 37, further comprising:

means for repeating, for each comparator in said array, said adjustment step; and

registers for storing, for each comparator in said array, an offset calibration coefficient representing the average of several digital ramp signal values that invert its logical output state.

41. (New) The system of claim 28, further comprising means for storing, for each comparator in said array, said offset calibration value externally at A/D converter power-down for later retrieval at A/D converter startup.

42. (New) An A/D converter including at least one comparator array for flash A/D conversion of an analog signal, comprising:

means for providing, for each comparator in said array, a common reference signal to both comparator input terminals;

means for forcing each comparator in said array into the same predetermined logical output state; and

means for adjusting, for each comparator in said array, the comparator trip-point until the logical output state is inverted.

43. (New) The converter of claim 42, further comprising means for adjusting each comparator trip-point by a monotonically varying signal.

44. (New) The converter of claim 42, further comprising means for simultaneously adjusting all comparators in said array by a common ramp signal.

45. (New) The converter of claim 42, further comprising means for D/A converting, for each comparator in said array, a digital ramp signal into an analog trip-point adjustment signal.

46. (New) The converter of claim 45, further comprising registers for storing, for each comparator in said array, an offset calibration coefficient representing the digital ramp signal value that inverts its logical output state.

47. (New) The converter of claim 45, further comprising registers for storing, for each comparator in said array, an offset calibration coefficient representing the average of an increasing digital ramp signal value that inverts its logical output state and a decreasing digital ramp signal value that inverts its logical output state.

48. (New) The converter of claim 45, further comprising means for repeating, for each comparator in said array, said adjustment step; and

registers for storing, for each comparator in said array, an offset calibration coefficient representing the average of several digital ramp signal values that invert its logical output state.

49. (New) The converter of claim 46, further comprising means for storing, for each comparator in said array, said offset calibration value externally at A/D converter power-down for later retrieval at A/D converter startup.

50. (New) The converter of claims 42, wherein the comparators in said array comprise regenerative latches.